Carbon Nanotube Field-Effect Transistors for Use as Pass Transistors in Integrated Logic Gates and Full Subtractor Circuits

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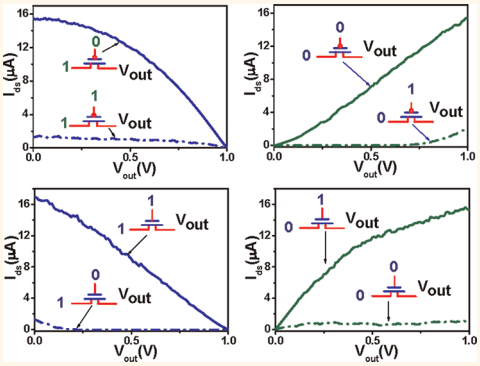
ABSTRACT



The use of carbon nanotube (CNT)-based field-effect transistors (FETs) as pass transistors is investigated. Logic gates are designed and constructed with these CNT FETs in the pass-transistor logic (PTL) style. Because two of the three terminals of every CNT FET are used as inputs, the efficiency per transistor in PTL circuits is significantly improved. With the PTL style, a single pair of FETS, one n-type and one p-type, is sufficient to construct high-performance AND or OR gates in which the measured output voltages are consistent with those quantitatively derived using the characteristics of the pair of the constituent n- and p-FETs. A one-bit full subtractor, which requires a total of 28 FETs to construct in the usual CMOS circuit, is realized on individual CNTs for the first time using the PTL style with only three pairs of n- and p-FETs.

KEYWORDS: carbon nanotube · logic gates · pass-transistor logic · integrated circuits · subtractor

The carbon nanotube (CNT) is considered to be one of the most promising building blocks for future integrated circuits (ICs) because of its excellent electrical properties, in particular, its high mobility, ultrasmall size, long mean free path length, and excellent thermal and mechanical properties. These properties make CNTs an ideal building material for high-performance field-effect transistors (FETs).[1−3] In the past decade, FETs built on individual CNTs have been pushed to their performance limits, both for p-type[4,5] and n-type[6−8] devices, by optimizing the source/drain contact materials and the gate structure,[4−8] and many basic logic gates and ring oscillators based on CNT FETs have been realized successively.[9−14] However, more advanced arithmetic circuits, which are extensively used in modern ultra-large-scale integrated circuits (VLSI) applications, have seldom been realized on individual CNTs. This is mainly because the yield of CNT-based devices is still very low, owing to the immaturity of the processes used for fabricating the CNT circuits. It is well-known that constructing relatively complex arithmetic circuits, such as a full adder/subtractor, when designed in the conventional CMOS style, requires more than 20 transistors,[14−16] and this is still a large number for the current fabrication processes used for individual CNTs. However, several integrated circuits with more complex functions and devices have been realized on CNT networks.[15−17] While the functions of these circuits are not expected to be comparable with those of Si-based circuits, these CNT network-based circuits are promising for flexible electronic applications.

To realize high-speed ICs with a high density, FETs fabricated on individual CNTs are preferred.[18] To demonstrate and explore arithmetic circuits on individual CNTs, efforts should be focused at the architectural level to improve the efficiency of every transistor and thus reduce the required number of transistors for the desired functions.[19−21] In the conventional CMOS design style, a power source is applied between the source and the drain of the

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FET, and only the gate electrode is used to input logic signals. However, when the FET functions as a pass transistor, in which two of the three terminals can be used to input signals, the efficiency per FET is at least doubled. Therefore, if the circuit can be designed with the pass-transistor logic (PTL) configuration, the number of transistors can be greatly reduced compared with the number needed for the usual CMOS configuration. Recently, CNT FET-based integrated circuits were designed in the PTL style, and several logic and arithmetic circuits were realized with significantly reduced numbers of transistors.[22] However, it was not clear how to quantitatively predict the behavior of the PTL logic gate from the electronic characteristics of its constituent FETs. Moreover, arithmetic functions other than a full adder were not realized, limiting the construction of more complex integrated circuits.

In this paper, we explore the pass-transistor operation of CNT-based p-type and n-type FETs. Basic CNT-based AND and OR gates are constructed with the PTL style. The measured output voltage levels are quantitatively analyzed and then found to be consistent with the results that were obtained using the output characteristics of the constituent n- and p-type CNT FETs. Using the PTL style, a CNT-based one-bit full subtractor, which requires 28 FETs to construct in the usual CMOS circuit, is realized with only three pairs of n- and p-type CNT FETs.

RESULTS AND DISCUSSION

CNT-based p-type and n-type FETs were fabricated with a self-aligned top-gate structure using a well-developed doping-free process that had been demonstrated and used in previous work.[6,7,12] Diagrams of the structures of the FET devices are shown in Figure 1a, and the SEM image in Figure 1b shows the fabricated devices and the integrated circuits that were tested to demonstrate the operation of pass-transistor logic. The operational principles of CNT FETs operating as pass transistors are demonstrated based on the experimental data shown in Figure 1c−f. When an FET operates as a pass transistor, two input logic signals can be supplied, one each to the source and the gate electrodes. Thus, there are in total four combinations of logic inputs to the source and the gate: (0, 0), (0, 1), (1, 0), and (1, 1). For all measurements presented in this paper, the devices and the circuits were supplied with a single voltage of 1.0 V; that is, the high voltage level representing "1" is 1.0 V, and the low voltage level representing "0" is GND. The p-type FET is first demonstrated as a pass transistor in Figure 1c,d, in which four distinct output characteristics are shown, corresponding to the different input combinations. When the logic value 1 is applied to the gate, the p-FET will be closed, and its output properties are shown by the dotted curves in Figure 1c,d. Among all four input combinations to the source and the drain, for the two corresponding to the situation in which "1" is applied to the gate (*i.e.*, (1, 1) and (0, 1)), the output current is very small (because the device is in the "off" state), regardless of the voltage applied to the source. In contrast, if the logic value 0 is applied to the gate, the enhanced p-FET will be open, and the corresponding output characteristics are shown in Figure 1c,d by the solid curves. In addition to the voltage applied to the gate, the output characteristics are additionally affected by the voltage applied to the source. The output characteristics for the input combination (1, 0) are thus different from those for (0, 0). Figure 1d shows clearly that $I_{ds}-V_{out}$ is linear as V_{out} approaches 1 V for the input combination (1, 0), suggesting that the signal "1" at the source can be well transferred to the drain. This is because most segments of the CNT channel are gated with a negative voltage of approximately −1.0 V, which is much smaller than the threshold voltage of the p-FET, yielding a small channel resistance. However, for the input combination (0, 0), $I_{ds}-V_{out}$ is nonlinear as V_{out} approaches 0 V, suggesting that the signal "0" at the source is not perfectly transferred to the drain. At this bias condition, most segments of the CNT channel are gated with 0 V, which is slightly higher than the threshold voltage of the p-FET. Because the p-FET is not completely open, the channel resistance is thus larger than that when passing a "1".

The operating principle of the n-type FET functioning as a pass transistor is similar to that of the p-type FET, but in a complementary way. The n-type pass transistor is turned off when the logic value "0" is biased on the gate, and this corresponds to the input combinations of (1, 0) and (0, 0) and the dotted curves in Figure 1e,f. In contrast, the n-FET is turned on when the logic value "1" is biased on the gate, and this corresponds to the input combinations of (1, 1) and (0, 1) and the solid curves in Figure 1e,f.

When an FET operates in conventional CMOS circuits, it is usually used as a switch and connected directly to the power supply;[21] that is, its source and drain terminals are biased with the power supply. Only the gate electrode is used to input a logic signal. In contrast, when functioning as a pass transistor, the FET may be powered directly by the input signal.[19] In principle, two of the three terminals of an FET can be used for signal inputs, and the efficiency per device may be at least doubled. The advantage of the improved efficiency per device can be utilized in designing circuits to reduce the transistor number; that is, the circuit can be significantly simplified if FETs are used as pass transistors or with the PTL style.[19−22]

We now consider how transistors operate in basic logic gates designed with the PTL style. The PTL OR gate is examined first. The circuit design is shown as the equivalent circuit diagram in the inset of Figure 2a, in which only an n-type and a p-type CNT FET are used. The measured output voltages for all four input combinations,

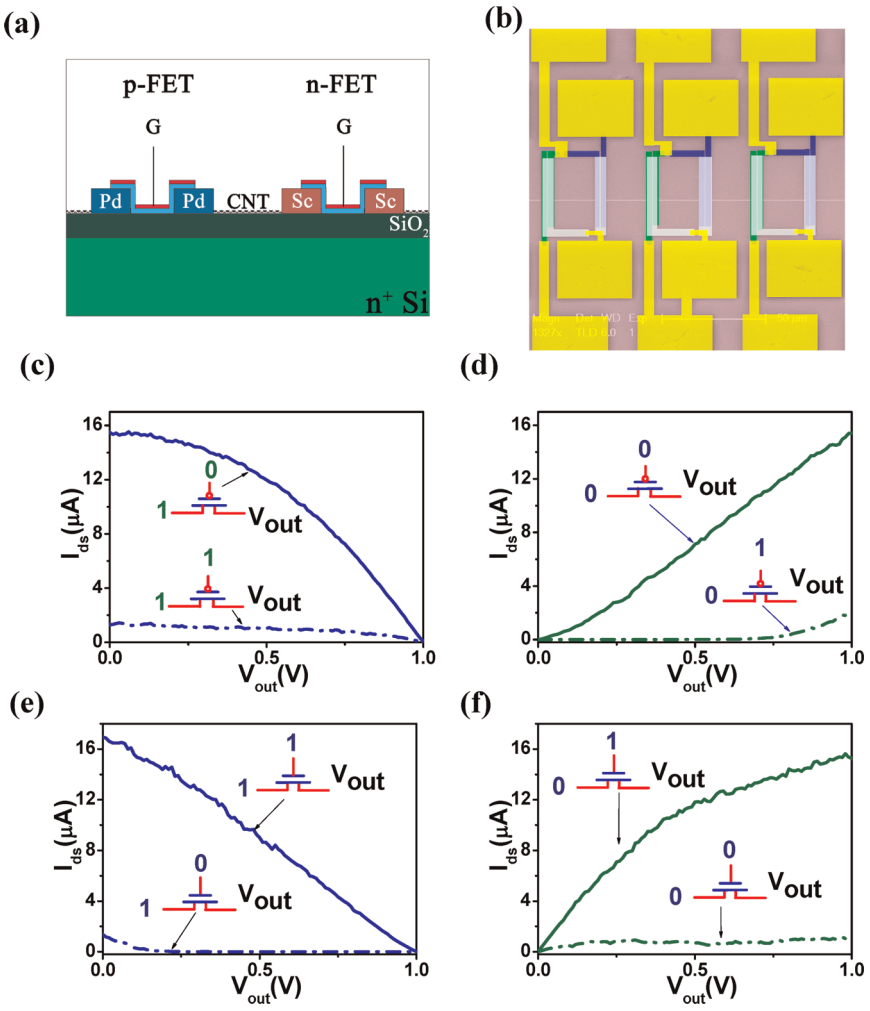


Figure 1. Structure and characteristics of CNT-based FETs. (a) Schematic diagram showing a side view of SWCNT-based CMOS devices with a p-FET/n-FET pair. (b) SEM image showing CNT CMOS devices and circuits fabricated on a semiconducting SWCNT with a diameter of approximately 2.2 nm. Output characteristics of a p-type pass transistor for input signal combinations on the source and the gate of (c) (1, 1) (dotted curve) and (1, 0) (solid curve), and of (d) (0, 1) (dotted curve) and (0, 0) (solid curve). Output characteristics of an n-type pass transistor for input signal combinations on the source and gate of (e) (1, 0) (dotted curve) and (1, 1) (solid curve) and (f) of (0, 0) (dotted curve) and (0, 1) (solid curve).

which follow the standard OR logic functions with nearly exact "1" and "0" levels, are shown in Figure 2a. Among the four outputs, the ones corresponding to the input combinations (0, 0) and (1, 1) are exact. The outputs for the other two input combinations (0, 1) and (1, 0) are slightly degraded; both of the outputs show voltage levels centered on 0.98 V (see Figure 2b). The output voltage of the OR gate can be deduced from the characteristics of its constituent FETs as the intersection of these output characteristics. For example, when inputting (A, B) = (0, 1), the p-FET is biased with 0 on its source and 1 on its gate (denoted here as (0, 1)), and the n-FET is biased with (1, 1). The output voltage is determined by the intersection of the output characteristics of the p-FET (biased with (0, 1) and denoted with a dotted line) and the n-FET (biased with (1, 1) and denoted with the solid line), as shown in Figure 2c. The derived output voltage was approximately 0.97 V, which agrees well with the measured value of 0.98 V. When inputting (A, B) = (1, 0) to the OR gate, the p-FET works with a bias of (1, 0), and the n-FET works under a bias of (0, 0). The output voltage was determined to be approximately 0.97 V from the intersection of the output characteristics of the p-FET (biased with (1, 0)) and the n-FET (biased with (0, 0)), as shown in Figure 2d. The derived output voltage was very close to the measured values of approximately 0.98 V, as well. In a similar way, the output voltage for the input combinations (0, 0) and (1, 1) can be analyzed as well through the output characteristics of the p- and n-FETs under corresponding bias conditions. Again, the output voltage values agreed well with those measured experimentally; they are very close to "0" and "1".

The circuit diagram of a PTL AND gate additionally consists of a pair of CNT FETs, one n-type and one p-type, as shown in the inset of Figure 3a. The measured output voltages for all four input combinations are shown in Figure 3a and follow the standard AND logic functions. The output voltages for the input combinations (0, 0) and (1, 1) are exact, while those

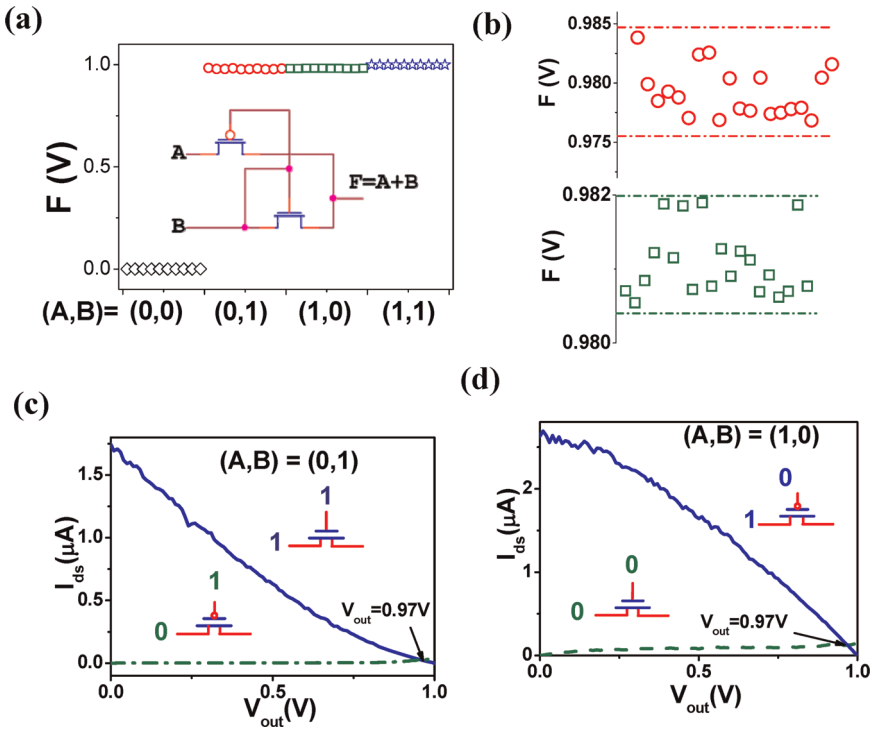


Figure 2. CMOS-based pass-transistor OR gate. (a) Output voltage levels for all four input combinations of the OR gate. Inset: circuit diagram. (b) Measured output voltage distribution for input combinations of (0, 1) (top) and (1, 0) (bottom). (c) Output voltage level analysis for input combinations of (A, B) = (0, 1), in which the p-FET is biased with (0, 1) on the source and the gate (dotted curve) while the n-FET is biased with (1, 1) (solid curve). (d) Output voltage level analysis for input combination of (A, B) = (1, 0), in which the p-FET is biased with (1, 0) (solid curve) and the n-FET is biased with (0, 0) (dotted curve). Both transistors were fabricated on the same semiconducting CNT with a diameter of approximately 1.4 nm.

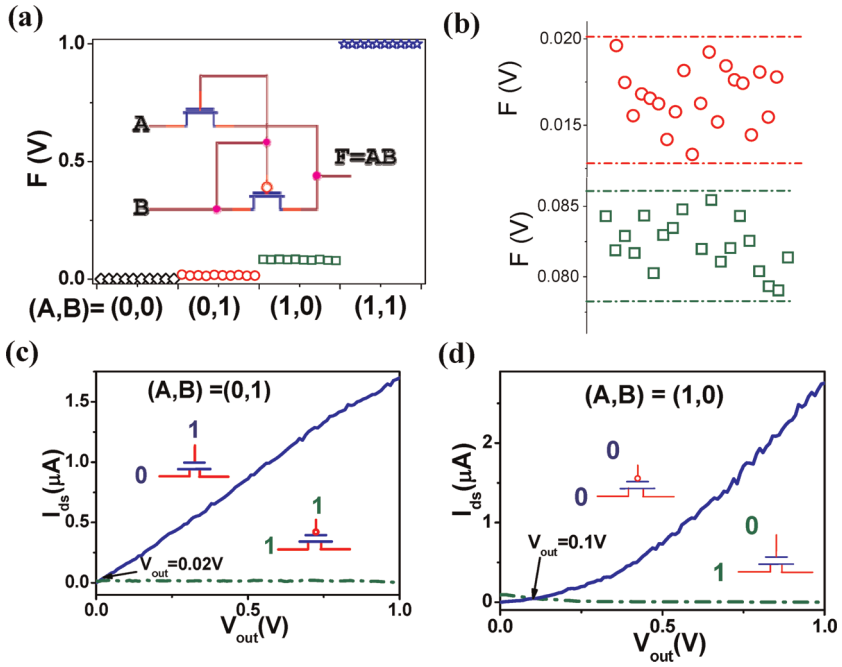
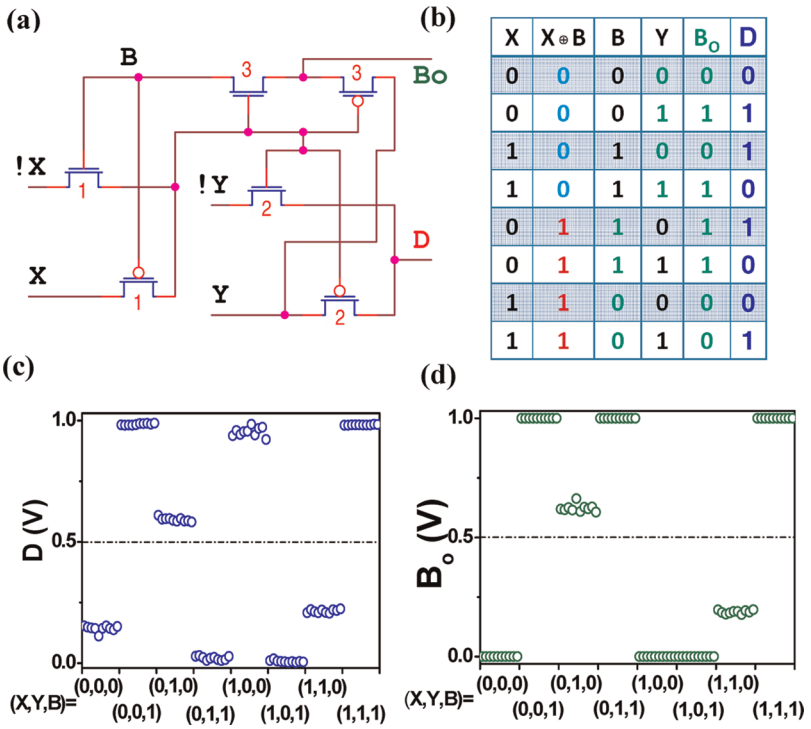


Figure 3. CMOS-based pass-transistor AND gate. (a) Output voltage levels for all four input combination of the AND gate. Inset: circuit diagram. (b) Measured output voltage distribution for input combinations of (A, B) = (0, 1) (top) and (1, 0) (bottom). (c) Output voltage level analysis for input combination (0, 1), in which the n-FET is biased with (0, 1) on the source and the gate (solid curve) and the p-FET is biased with (1, 1) (dotted curve). (d) Output voltage level analysis for input combination (1, 0), in which the n-FET is biased with (1, 0) on the source and the gate (dotted curve) and the p-FET is biased with (0, 0) (solid curve). Both transistors were fabricated on a semiconducting CNT with a diameter of approximately 1.4 nm.



X	X⊕B	B	Y	B_0	D
0	0	0	0	0	0
0	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	1	0
0	1	1	0	1	1
0	1	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	1

Figure 4. CNT-based full subtractor designed with the pass-transistor logic style. (a) Circuit design for a full subtractor, where *D* denotes difference and B_0 denotes borrow. (b) Truth table of the full subtractor. (c) Output voltage levels of the subtractor for *D* and all eight input combinations of (X, Y, B), and (d) corresponding output voltage levels for B_0 and all eight inputs.

for (0, 1) and (1, 0) are slightly degraded at 0.02 and 0.08 V, respectively, for the two inputs (see Figure 3b). Similarly, the output voltage is determined by the intersection of the output characteristics of the two constituent FETs as in the case of the OR gate, and this is because the n- and p-type FETs share the same drain or output voltage. For the input combination (A, B) = (0, 1), the p-FET in the AND gate is biased with (1, 1) on the source and gate, while the n-FET is biased with (0, 1). The output voltage is determined by the intersection of the output characteristics of the p-FET [biased with (1, 1)] and the n-FET [biased with (0, 1)], as shown in Figure 3c. The derived output voltage was approximately 0.02 V, which is very close to the measured value. When inputting (A, B) = (1, 0), the p-FET is biased with (0, 0), and the n-FET is biased with (1, 0). The output voltage was approximately 0.1 V, as determined from the intersection of the output characteristics of the p-FET at (0, 0) and the n-FET at (1, 0), as shown in Figure 3d. The derived output voltage was close to the measured value of 0.08 V, which differed slightly from the logic value "0" (0 V). This error originates from the nonideal signal transfer associated with the p-type pass transistor with (0, 0) (denoted by the blue solid curve in Figure 3d). In the same way, the output voltages for the input combinations (0, 0) and (1, 1) can be analyzed using the output characteristics of the constituent p- and n-FETs, and the output voltages were found to be very close to zero for (0, 0) and exactly one for (1, 1).

From the above demonstrations of PTL OR and AND gates, we can observe that the PTL circuits are indeed significantly simplified when FETs are used as pass transistors. Only two transistors are required for a PTL OR gate or AND gate, while six transistors are needed in a conventional CMOS-style design.[19] In principle, logic circuits of any complexity can be constructed based on AND and OR logic gates, accompanied with an inverter, so that significant savings on transistors can be expected for all digital ICs employing the PTL style.

A full subtractor is an important arithmetic circuit for performing subtraction with three inputs, for example, X (minuend), Y (subtrahend), and B (borrow in from a previous bit), and it outputs the difference, *D*, and borrow, B_0. If the conventional CMOS style is used to design a one-bit full subtractor, 28 transistors are required, which is a large number given the current technology and is difficult to achieve on individual CNTs. However, the predicament can be solved if every FET is used as a pass transistor. A one-bit full subtractor may be constructed by integrating three pairs of CMOS-based pass transistors; the equivalent circuit diagram is shown in Figure 4a. The full subtractor is designed based on the core XOR gate, which is composed of an n-FET and a p-FET.[22] The output of the first-stage XOR logic, X⊕B, composed of a pair of pass transistors labeled with a "1" in Figure 4a, is connected to the gate of another pair of pass transistors, labeled with a "3", to decide whether to pass input B or input Y to the borrow output B_0. Meanwhile, X⊕B is additionally

connected to the second stage of an XOR gate composed of two pass transistors labeled with a "2" to obtain the difference *D*. The difference *D*, which equals X − Y − B, can be expressed using the logic relation $D = [(X \oplus B) \oplus Y]$. To understand and verify the correctness of B_0, a truth table is shown in Figure 4b. When inputs X and B are equal (see the first four lines of Figure 4b), the output X⊕B is 0 (denoted by light blue zeroes). When inputs X and B are different (see the last four lines of the truth table), X⊕B is 1 (denoted by brown ones). The output B_0 is the same as the input Y in the first four lines of Figure 4b and is equal to the input B in the last four lines. According to the analysis given above, B_0 can be expressed as $Y[!(X \oplus B)] + B(X \oplus B)$. The result of X⊕B is just a switch that can determine the output of B_0, so the output of X⊕B is connected to the gate of the two pass transistors labeled with "3" in Figure 4a to choose the correct signal for B_0.

The measured output voltages for all eight input combinations of (X, Y, B) are shown in Figures 4c,d. *D* and B_0 for all eight input combinations agree exactly with the truth table of the full subtractor if we define voltage ranges between 0 and 0.23 V as the logic value "0" and those between 0.58 and 1 V as the logic value "1". Therefore, a full subtractor was successfully realized on a single CNT, and it benefited from the PTL circuit style. However, it should be noted that the output voltages for certain input combinations, such as (X, Y, B) = (0, 1, 0) for *D* and (1, 1, 0) for B_0, had larger errors than those for other inputs. The signal degradation mainly originates from fluctuations in the threshold voltages of the CNT FETs used in the circuit,[22] and the performance of these PTL circuits can be further improved by using transistors with uniform performance, which could be accomplished by optimizing the fabricating process.

It is worth noting that only six transistors are needed to construct a one-bit full subtractor with PTL, whereas 28 transistors are required in a conventional CMOS circuit design. Of course, two inverse signals, !X and !Y, were used in the PTL subtractor, which can be obtained from X and Y by adding two CMOS inverters. Therefore, 10 transistors are sufficient to construct a PTL one-bit full subtractor without requiring inverse signals, suggesting a savings of more than 64% in the transistor count compared with that using the CMOS style. The significant saving comes from the significantly improved efficiency when the pass transistor operating mode is used. In addition, it is well-known that the silicon FET-based PTL circuit is unstable, which is mainly caused by the signal degradation originating from the threshold voltage drop and the absence of gain.[19] In a CNT FET-based PTL circuit, this problem can be easily solved. This is because the threshold voltage drop is largely avoided because of the near-zero threshold voltage for both the n-FET and the p-FET.[22] In addition, a CMOS inverter with a gain larger than 1 can be readily cascaded at the output of the PTL gate to restore the degraded output signal.[22]

CONCLUSION

The output properties of CNT FETs operating as pass transistors were explored, and the CNT FETs were used to build logic circuits designed with the pass-transistor logic (PTL) style. Because two of the three terminals of each CNT FET can be used to input signals, the efficiency per transistor in PTL circuits is significantly improved. Using basic CNT-based AND and OR gates with the PTL style, the output voltage levels were measured and shown to be consistent with the levels obtained using the output characteristics of constituent n- and p-type CNT FETs. Using the PTL style, a one-bit full subtractor, which requires 28 FETs to construct in the usual CMOS circuit, was realized on individual CNTs for the first time with only three pairs of n-FETS and p-FETs.

METHODS

The CNTs used in this work were directionally grown on a silicon substrate,[23] and semiconducting single-walled CNTs were identified *via* field-effect measurements using the substrate as the back gate; these were used for further device fabrication. The p-type and n-type FETs with a self-aligned gate structure[7] were fabricated on the same CNTs through the doping-free CMOS FET process developed. The p-type FETs were fabricated first. A patterned Pd film with a thickness of 80 nm was used for fabricating the source and the drain contact electrodes *via* electron beam lithography (EBL), electron beam evaporation (EBE), and a subsequent standard lift-off process. Windows for gate stacks were then patterned *via* another EBL process, and gate stacks consisting of HfO_2/Pd with a thickness of 12 nm/10 nm were grown by atomic layer deposition (ALD) and EBE. An HfO_2 film with a dielectric constant of approximately 18 was grown at 90 °C. The p-type FETs were finished after a lift-off process for forming the stripes of the gate stacks. The n-type FETs were fabricated subsequently with fabrication processes similar to those used for p-type FETs, but Sc was used instead of Pd as the source and the drain contacts to form ohmic contacts to the CNT for electrons. It should be noted that the Sc film was evaporated under an ultrahigh base vacuum of up to 2×10^{-8} Torr to form high-performance n-type ohmic contacts to the CNT. In this work, a high work function metal, Pd, was employed for the gate electrode, both for the p-FETs and the n-FETs, to adjust the threshold voltage to be centered around zero and to ensure that the circuits can operate under a single low supply voltage.[7,12] It is well known that the main drawback of conventional Si-based PTL circuits is the threshold voltage drop resulting from different threshold voltages for n-type and p-type FETs. Because both the n- and p-type CNT pass transistors have threshold voltages near zero, the threshold voltage drops normally encountered in Si-based PTL circuits are avoided. Finally, a Ti/Au film was patterned and used for connecting wires to the n-type and p-type FETs for external measurements. Every FET was designed with three individual pads for the source, drain, and gate electrodes, which allowed simultaneous measurement and analysis of the performance of entire circuits and each constituent device. All devices and

circuits were measured in air using a probe station with a Keithley 4200 semiconductor analyzer and signal sources.

Conflict of Interest: The authors declare no competing financial interest.

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